Progress of 21CMA pulsar backend

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2025.7

21CMA & its pulsar backend

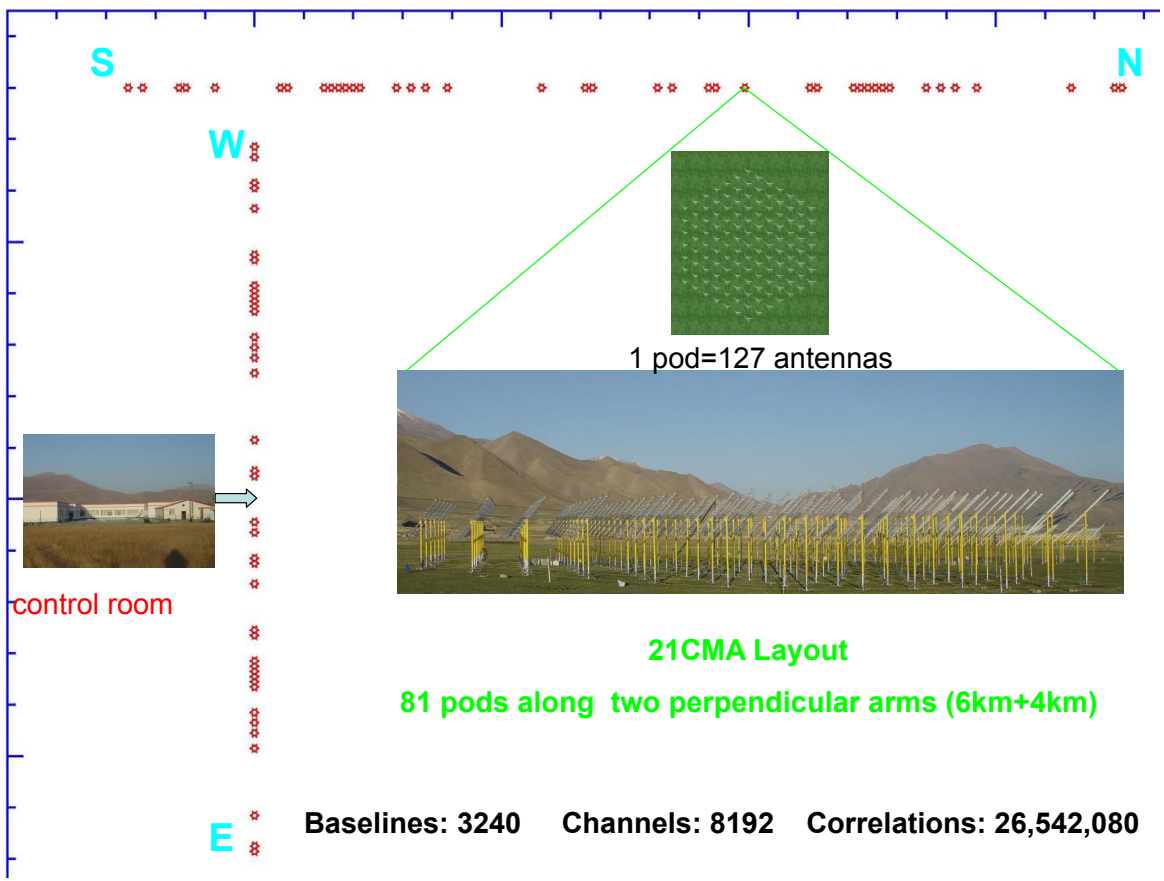


Figure 1: Location of stations of 21CMA (Zheng et al. 2015, 2016; Wu 2019)

21CMA & its pulsar backend

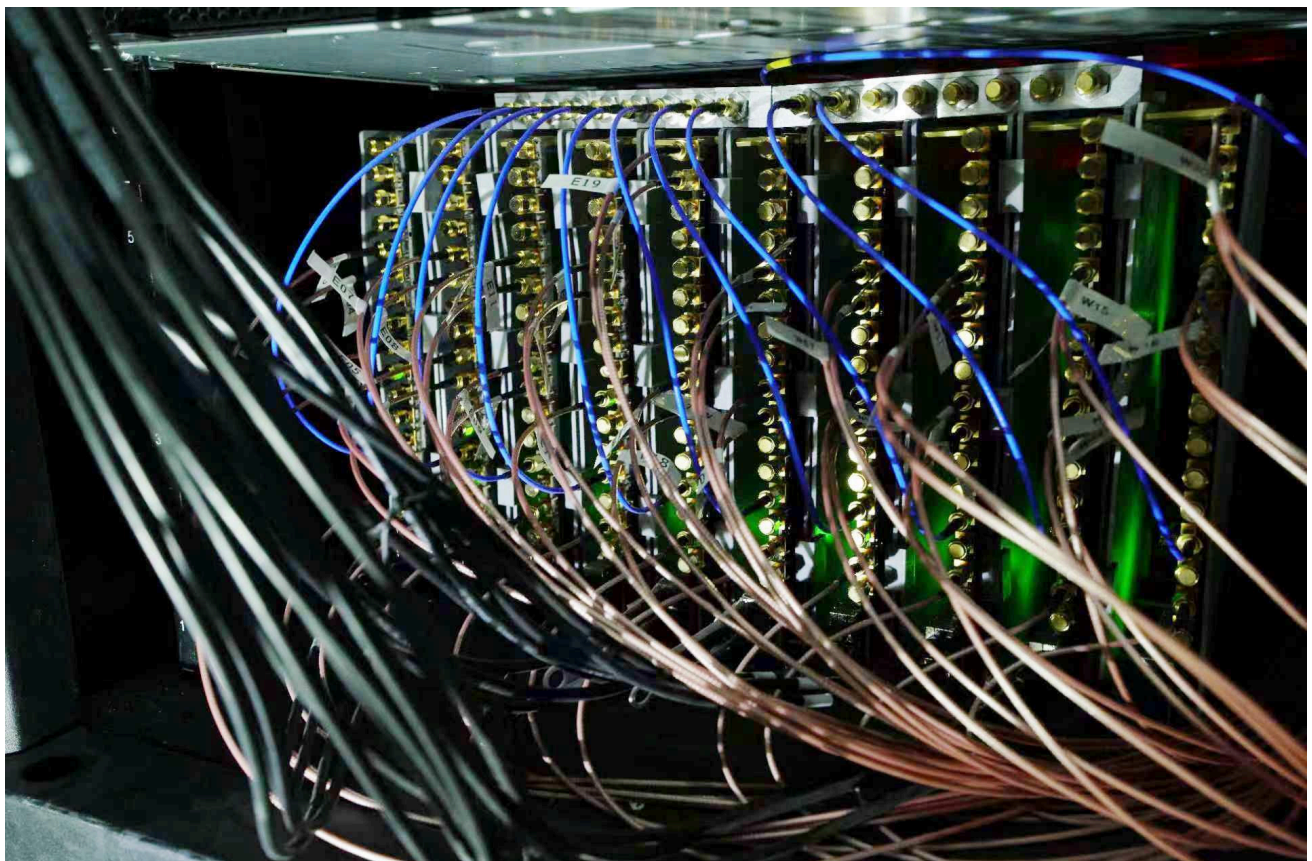


Figure 2: current 10 SNAP 1 v2 of 21CMA, image by Chunfeng Zhang

Correction of last FPS report: detection of pulsar

- detection of PSR B0329+54 reported last year not reproduced by other software
  - possibly caused by PulsarX command line `--rfi mask 1 1`
- re-observed using 21CMA Digital Beamforming (21CMA-DBF, **in single station**) backend (Gu and others 2025) (in prep.) at 2024.10.28, using E03 & W09
- convert single station auto-correlation into sigproc filterbank
- processed with PulsarX (Men et al. 2023a, 2023b), PRESTO (Ransom 2001, 2011) & DSPSR (Straten and Bailes 2011) + PSRCHIVE (Hotan et al. 2004) to verify that detection is real

PSR B0329+54 on single station (E03), 120 – 166 MHz

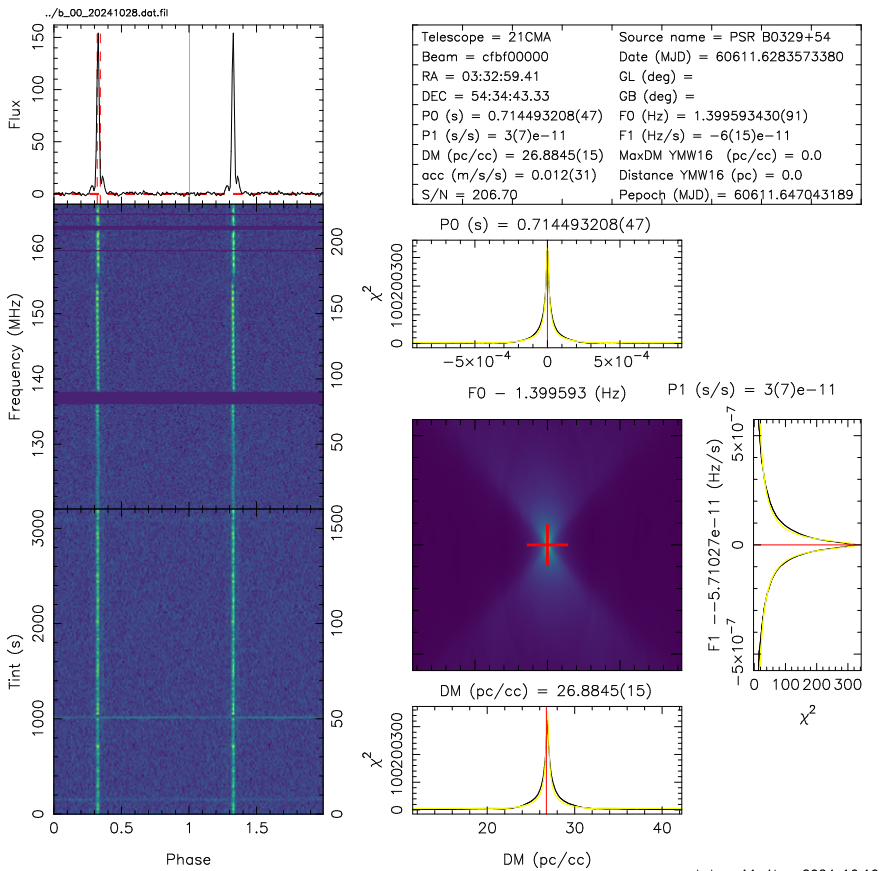


Figure 3: Processed by PulsarX

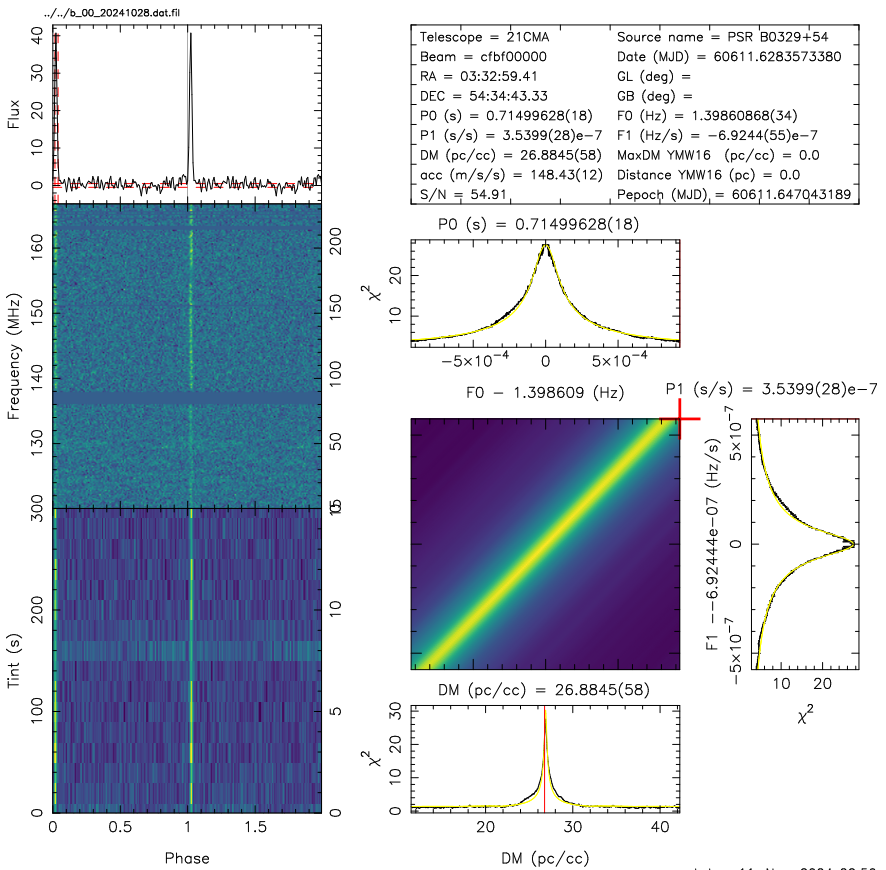


Figure 4: 5 min observation → S/N “54.9”

PSR B0329+54 on single station (E03), 120 – 166 MHz

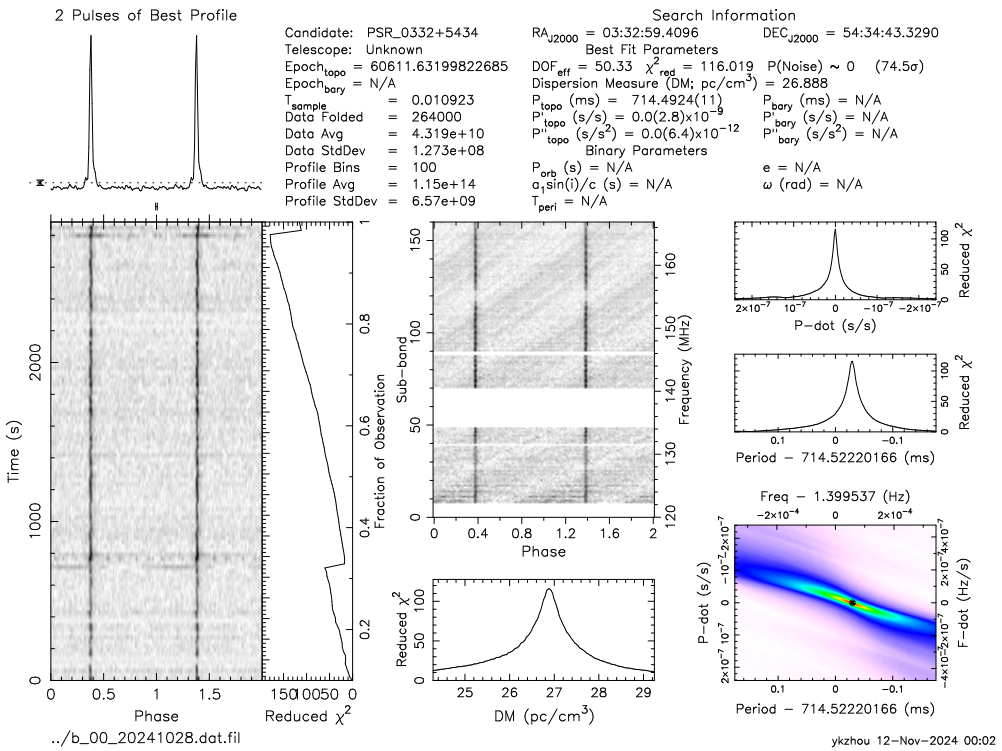


Figure 5: Processed by PRESTO

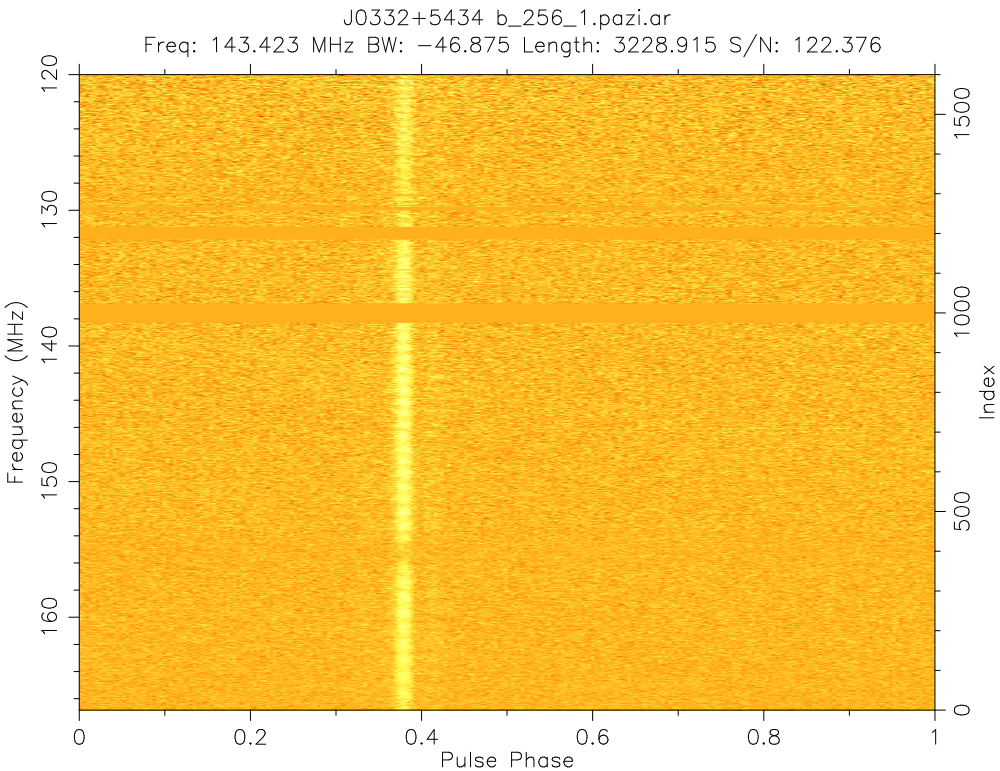


Figure 6: Processed by DSPSR + PSRCHIVE

PSR B0329+54 on single station (E03), 60 – 106 MHz & 150 – 192 MHz

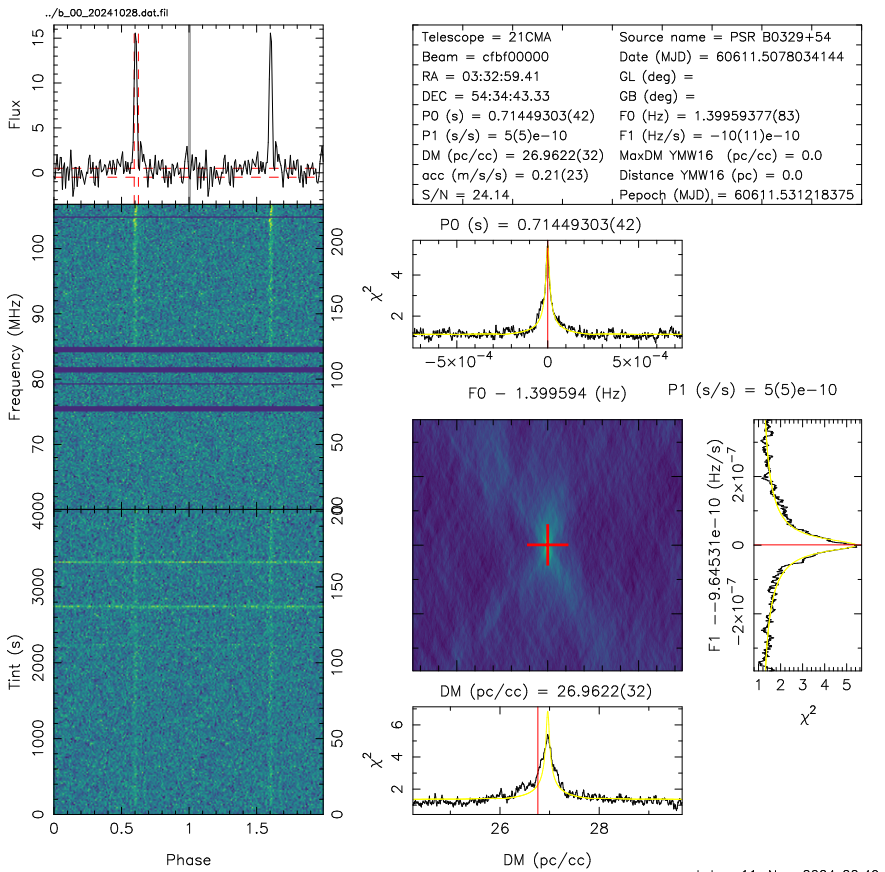


Figure 7: 60 – 106 MHz

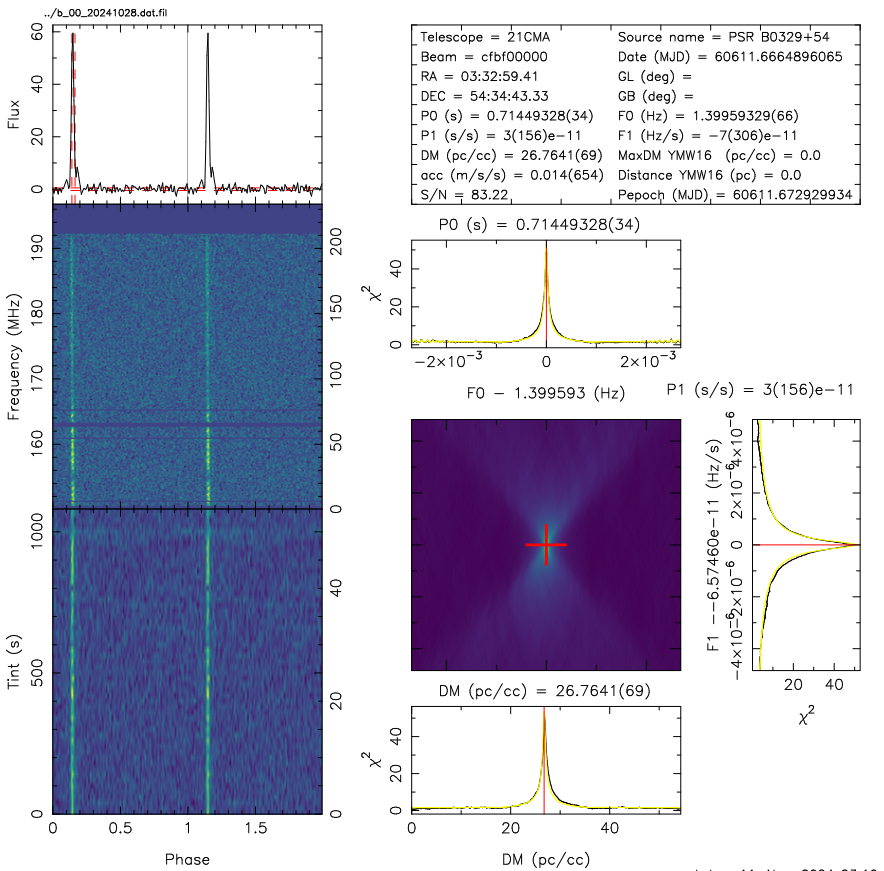


Figure 8: 150 – 192 MHz

GPU-based distributed Correlator

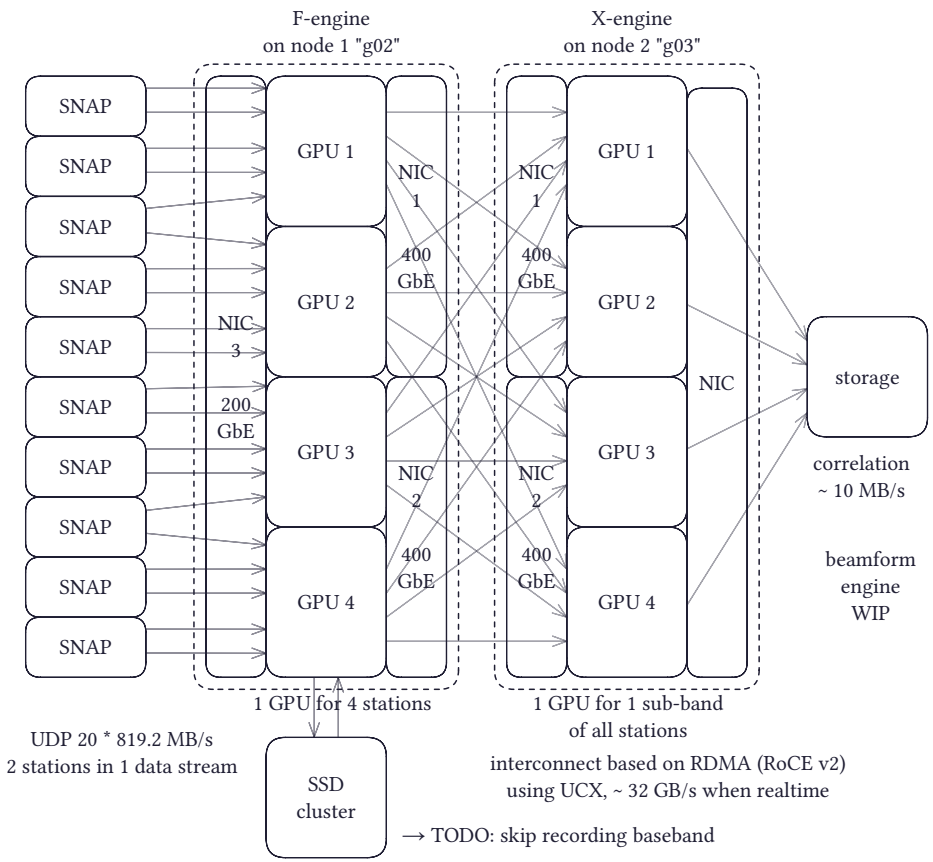


Figure 9: Data flow of correlator

- written in **SYCL 2020**, based on **AdaptiveCpp** (Alpay and Heuveline 2020, 2023), can run on **GPU from multiple vendors** including AMD, Hygon, NVIDIA, possibly Moore Threads, CPU from multiple vendors, and possibly other devices
- utilize Remote Direct Memory Access (RDMA) on Converged Ethernet (**RoCE v2**) using UCX (Shamis et al. 2015), 2×400 GbE interconnect
- Redis used as communication middleware
- input data rate: $20 \times (2 \times 409.6$ Msps)
- compute all baselines, all frequencies

GPU-based distributed Correlator

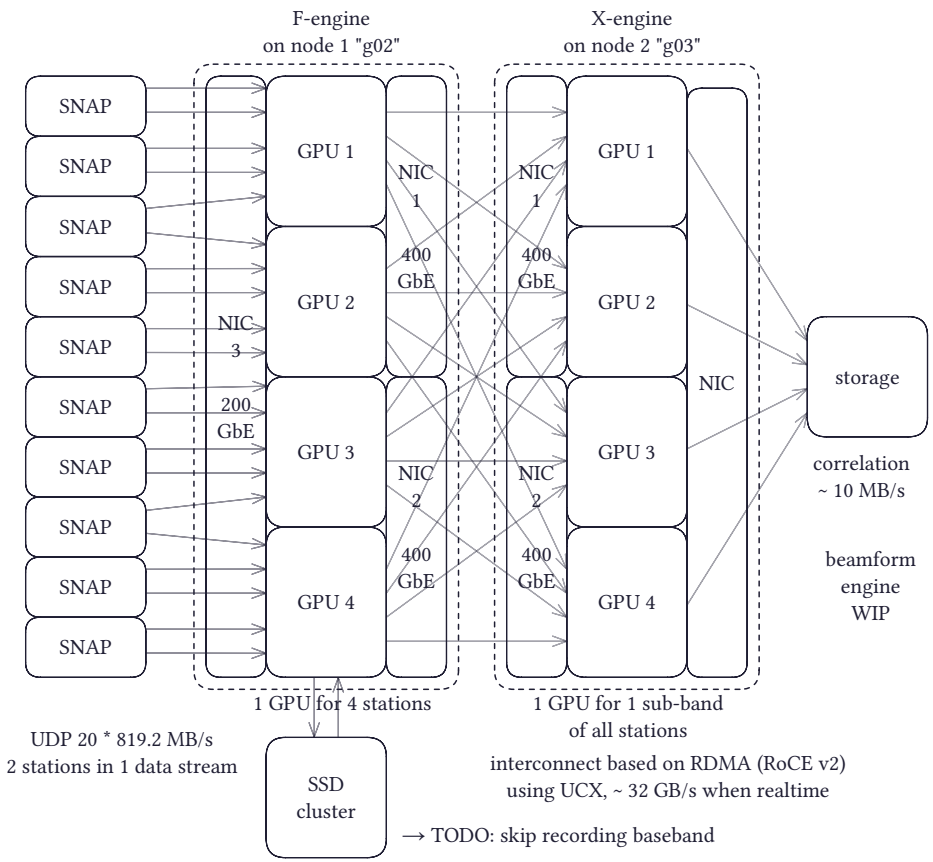


Figure 10: Data flow of correlator

- somewhere near “real-time”: observe and record data to SSD array at night for 12 h, process under daylight for < 12 h
  - severe RFI during daytime
- maybe capable of really real-time, not tested
- overall throughput:
  - GPU RDMA: **0.991x** (1x = realtime)
  - main RAM RDMA: **1.46x**
  - not sure what’s happening…
- detailed verification (imaging & calibration using e.g. CASA (The CASA Team et al. 2022)) working-in-progress
- code well open source when verified, collaboration welcome

GPU-based distributed Correlator

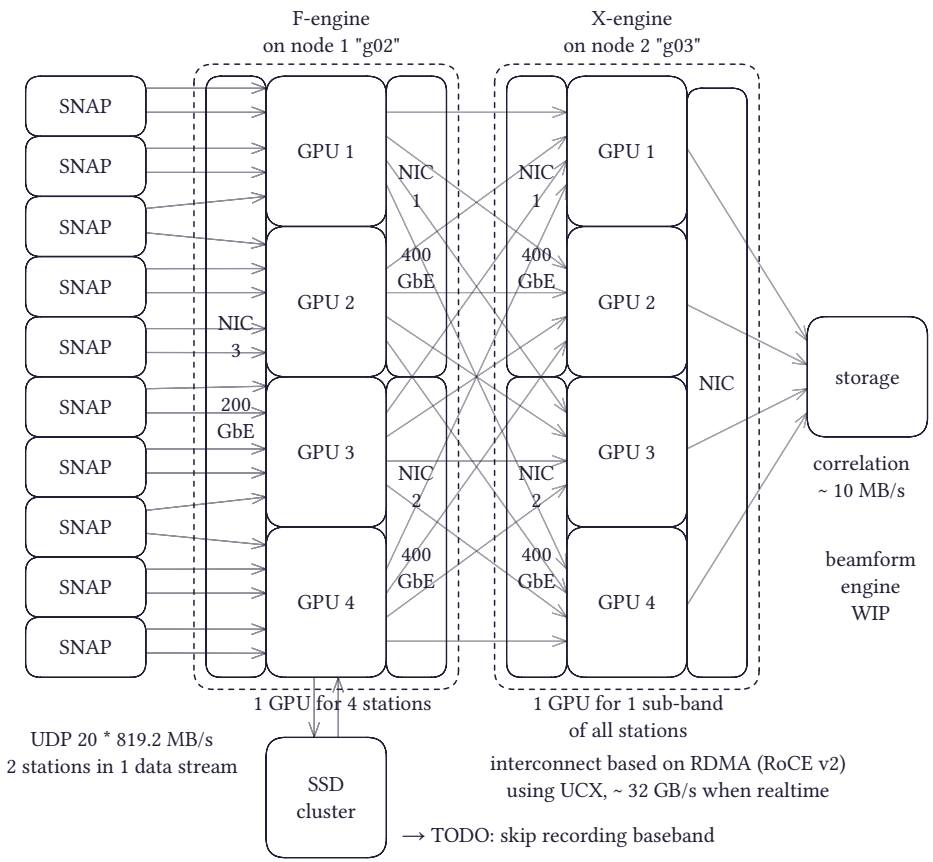


Figure 11: Data flow of correlator

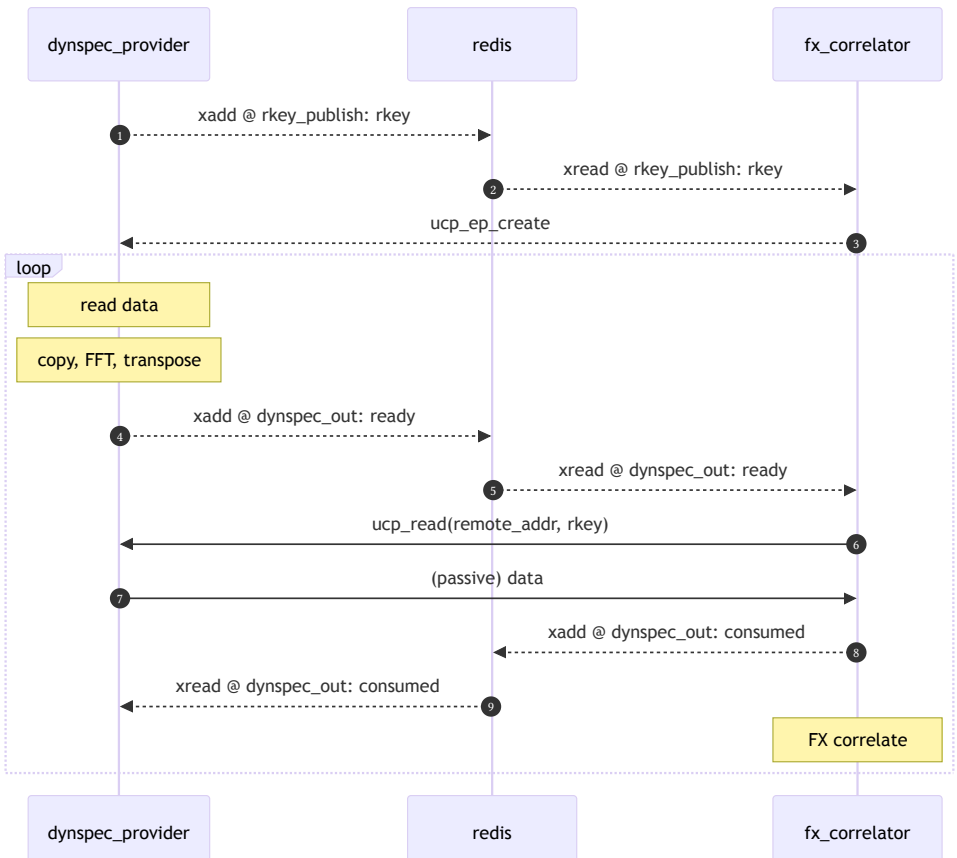


Figure 12: detailed F & X engine interconnect

GPU-based distributed Correlator

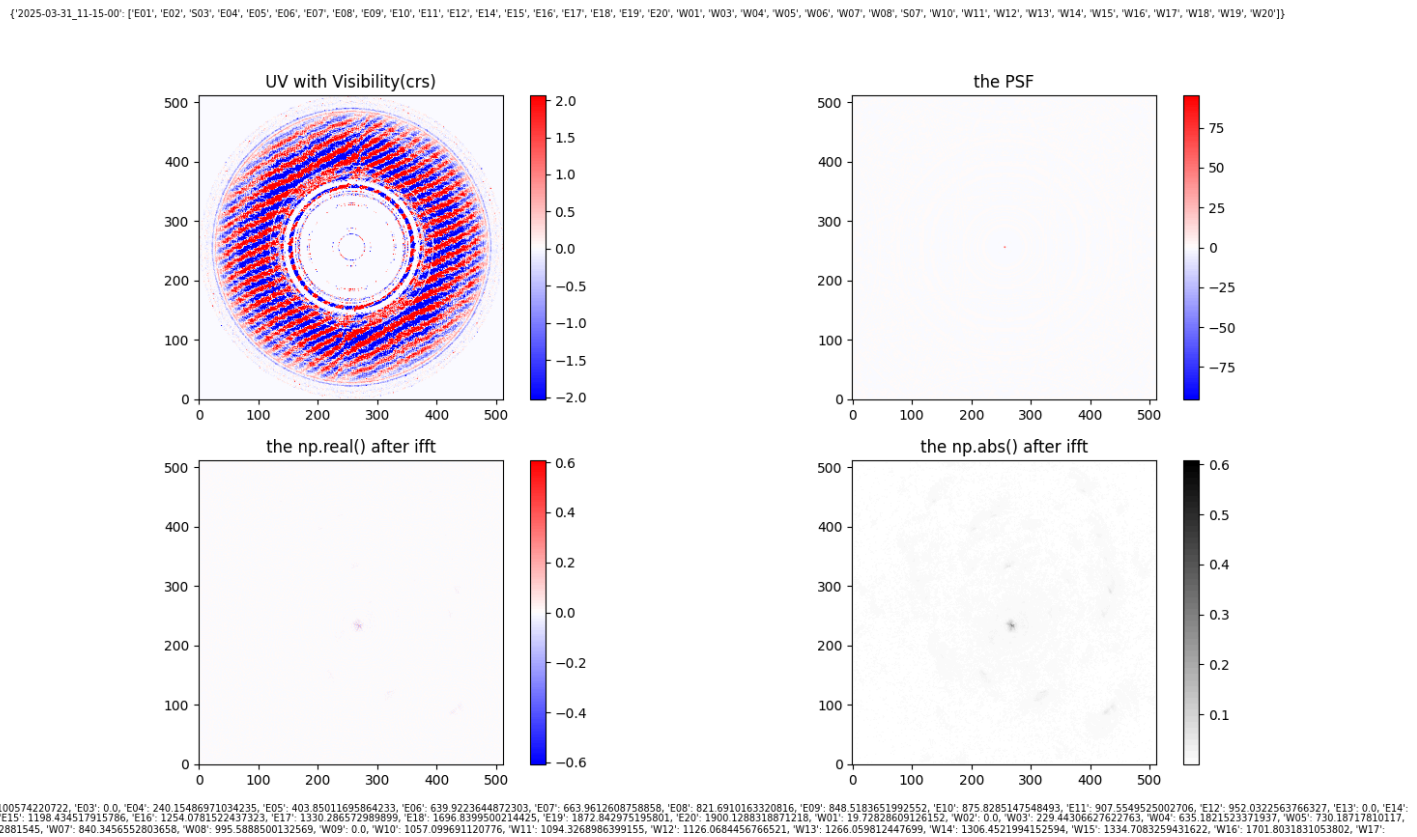


Figure 13: 50 – 200 MHz observation of north celestical pole using E & W arms + S07

GPU-based distributed Correlator

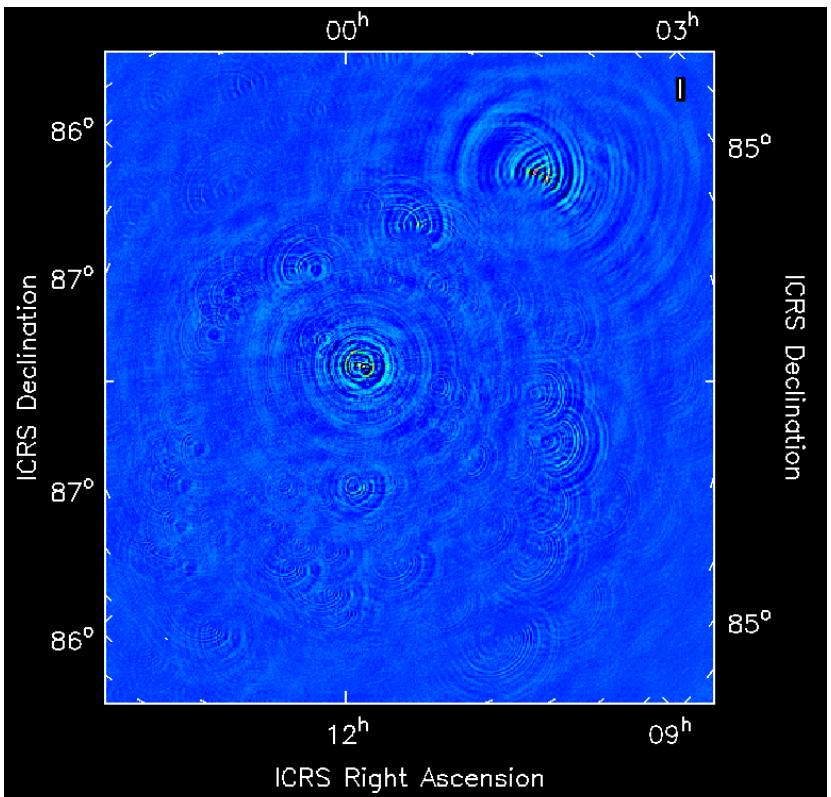


Figure 14: Dirty image of north celestical pole using CASA, all baselines

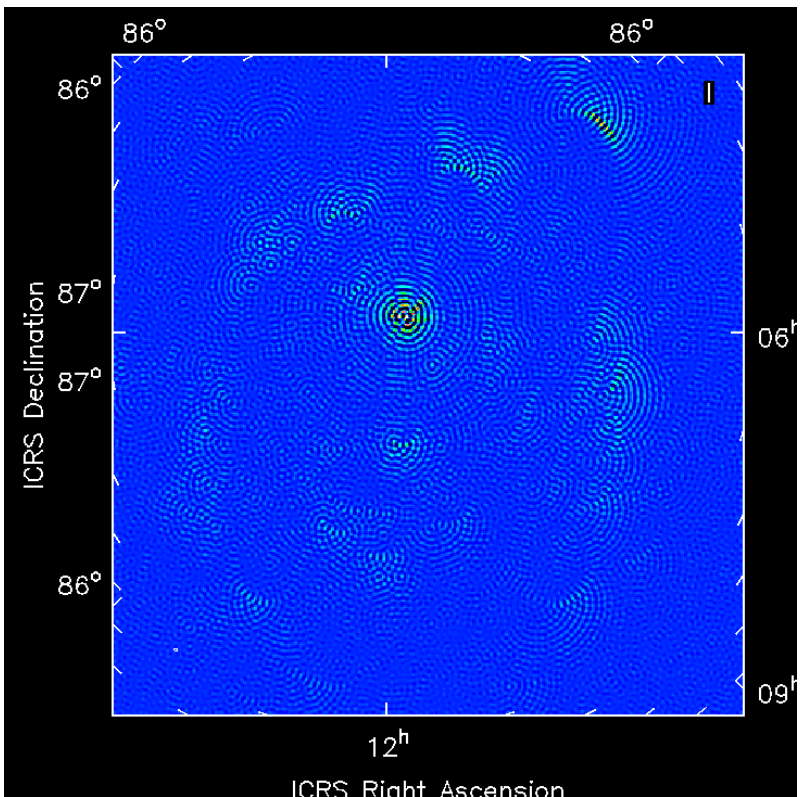


Figure 15: Dirty image of north celestical pole using CASA, E01-E20 baseline

Beamforming of two 21CMA-DBF stations (E03 + W09) (preliminary)

- observed PSR B0329+54 for $\sim$ 1 hour, simultaneously using E03 & W09, recorded baseband
- resample 21CMA-DBF "baseband" to SNAP 1 v2 "snapadc_direct1g"[1] baseband
- beamform **across stations** using self-written "21cma-make_beam"
  - MWA vcstools (Ord et al. 2019) & vcsbeam was used as a reference during coding
- E03 & W09: 1 kilometer east-west baseline
- folded output filterbank using PulsarX

[1] firmware written by Prof. Yan Zhu

Beamforming of two 21CMA-DBF stations (E03 + W09) (preliminary)

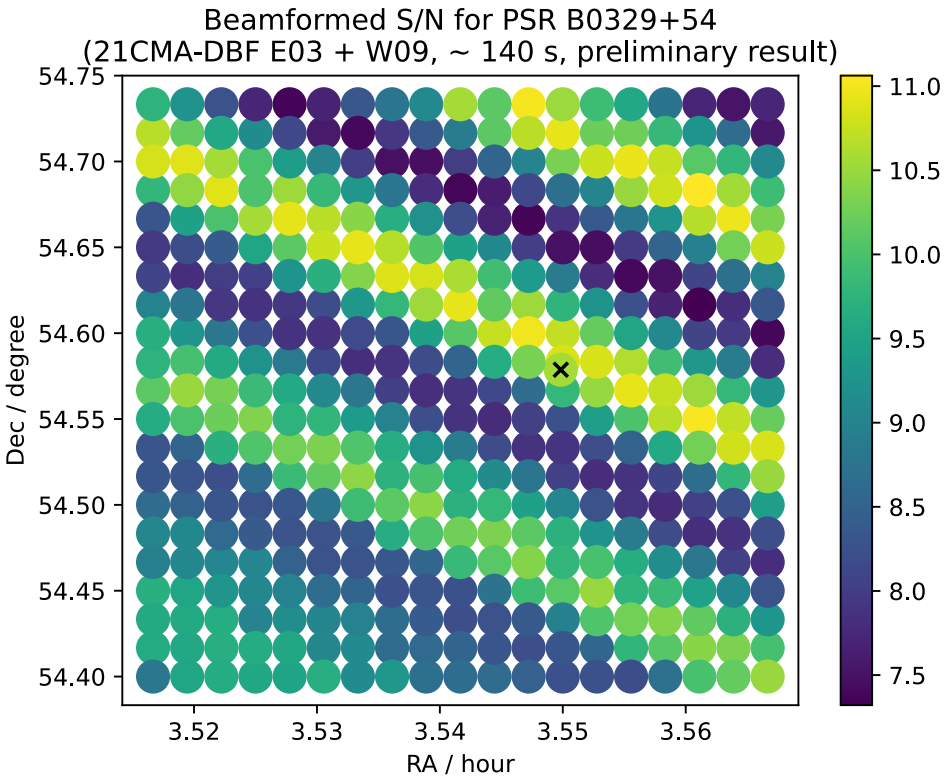


Figure 16: ~ 140 s observation, "×" = B0329+54

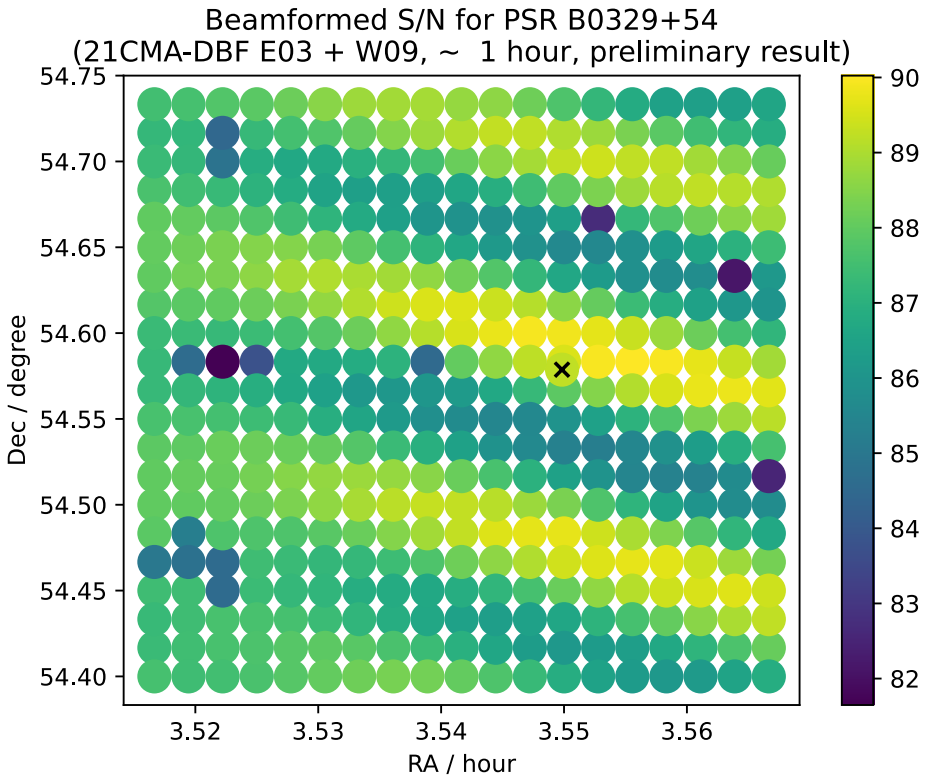


Figure 17: ~ 1 hour observation, "×" = B0329+54, RFI mitigation causes S/N outliers

Beamforming of two 21CMA-DBF stations (E03 + W09) (preliminary)

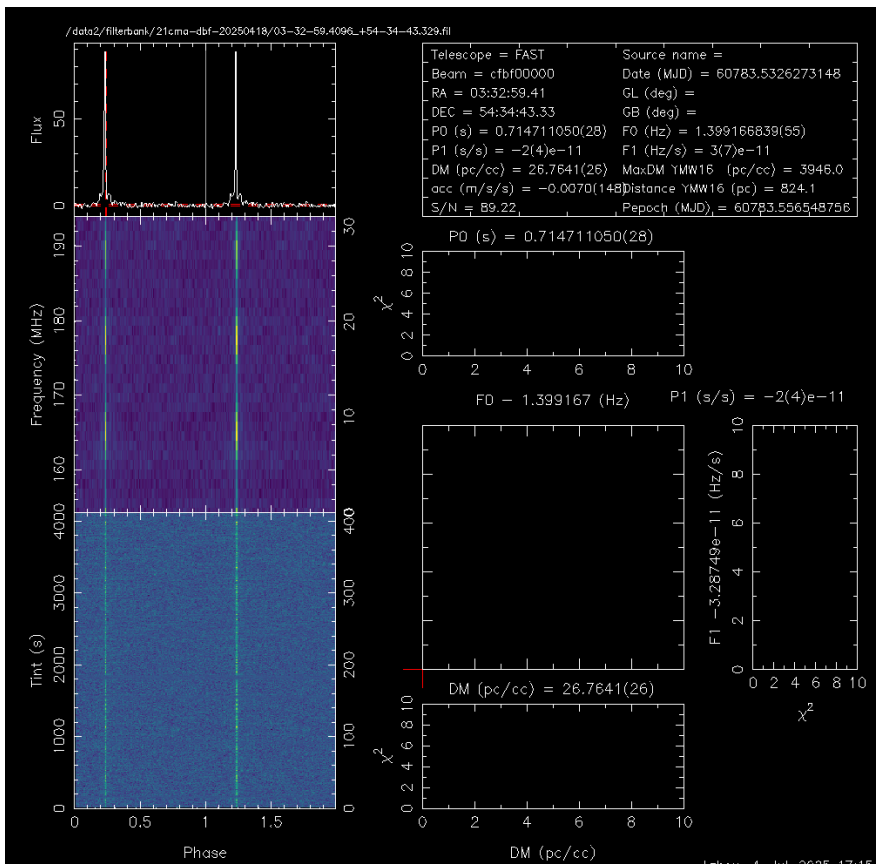


Figure 18: $\sim$ 1 hr obs. folded by PulsarX

- preliminary result
- details:
  - "telescope = FAST" because this unmodified PulsarX installation cannot recognize 21CMA
  - resampling from 21CMA-DBF baseband to SNAP 1 v2 "snapadc_direct1g" baseband causes a $\sim 2 \times 10^{-4}$ relative difference of P, which is expected

Sampling board: SNAP 1 v2

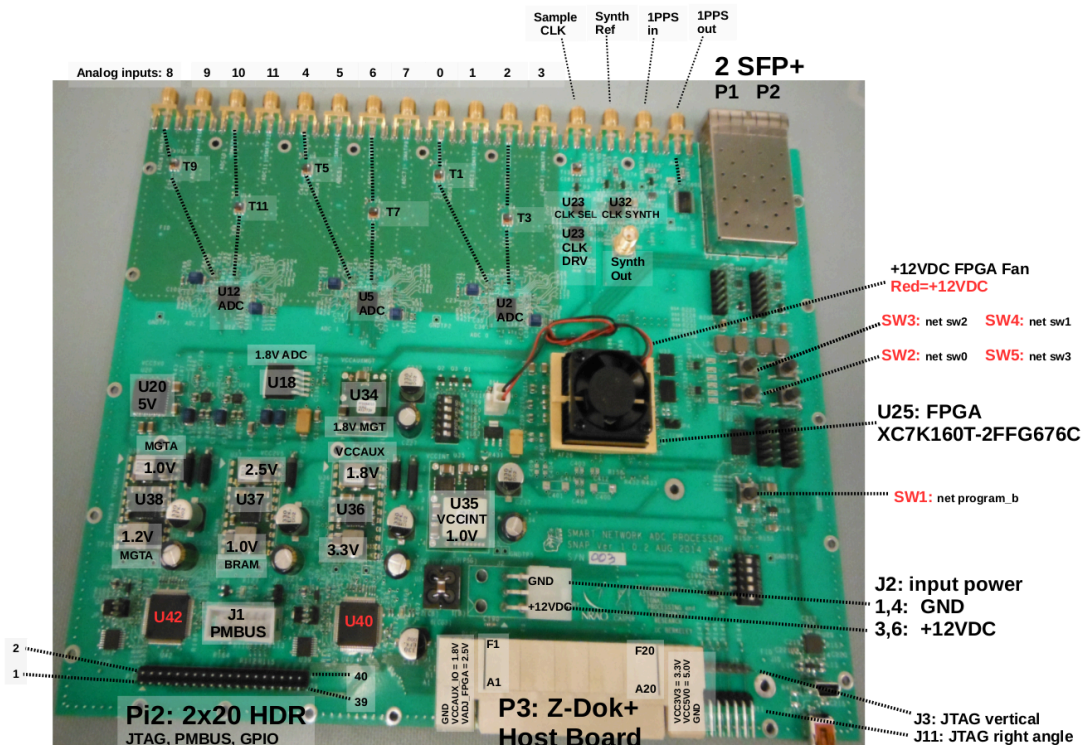


Figure 19: Overview of SNAP 1 v2 (DeBoer et al. 2020)

- currently used in 21CMA pulsar backend
- 3 × HMCAD1511, interleaved ADCs
- 2 × 10 GbE, mismatch with number of ADCs
- max data rate per board:
  - 8 × 250 Msps
  - 4 × 500 Msps
  - 2 × 1 Gsps
- interleaved ADC is related to unexpected phase jump ?
  - may be caused by incorrect reset of ADCs during power on ?

Sampling board: SNAP 1 v2

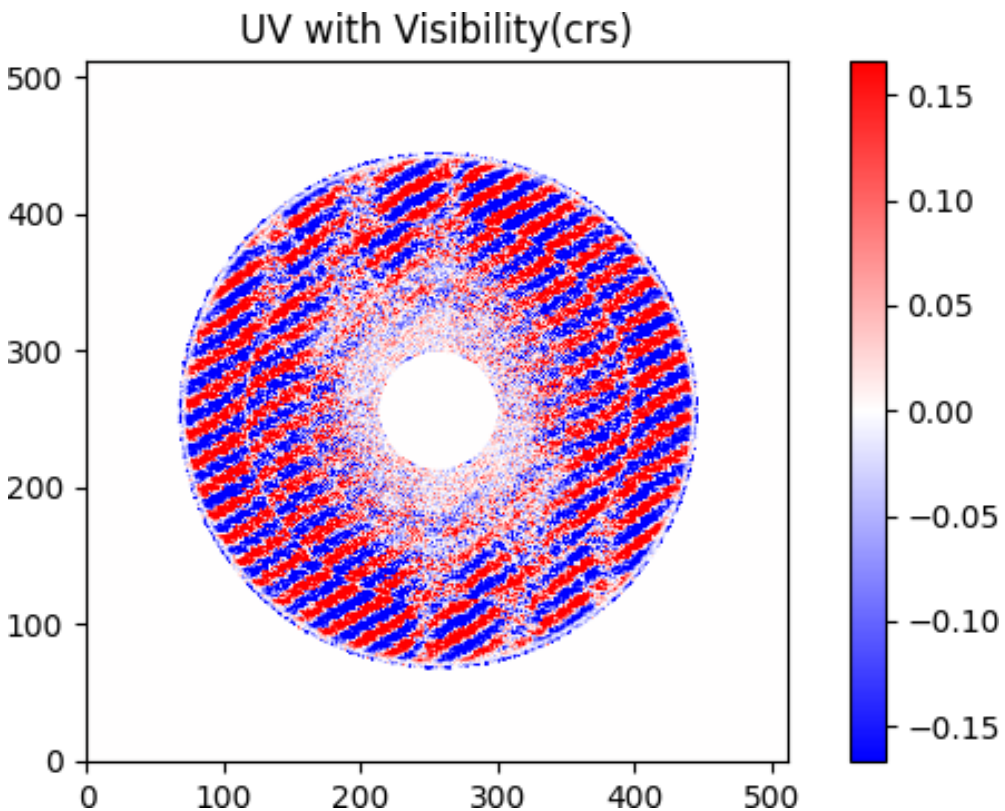


Figure 20: UV map of W20-E14, notice phase jump at 102.4 MHz & 153.6 MHz

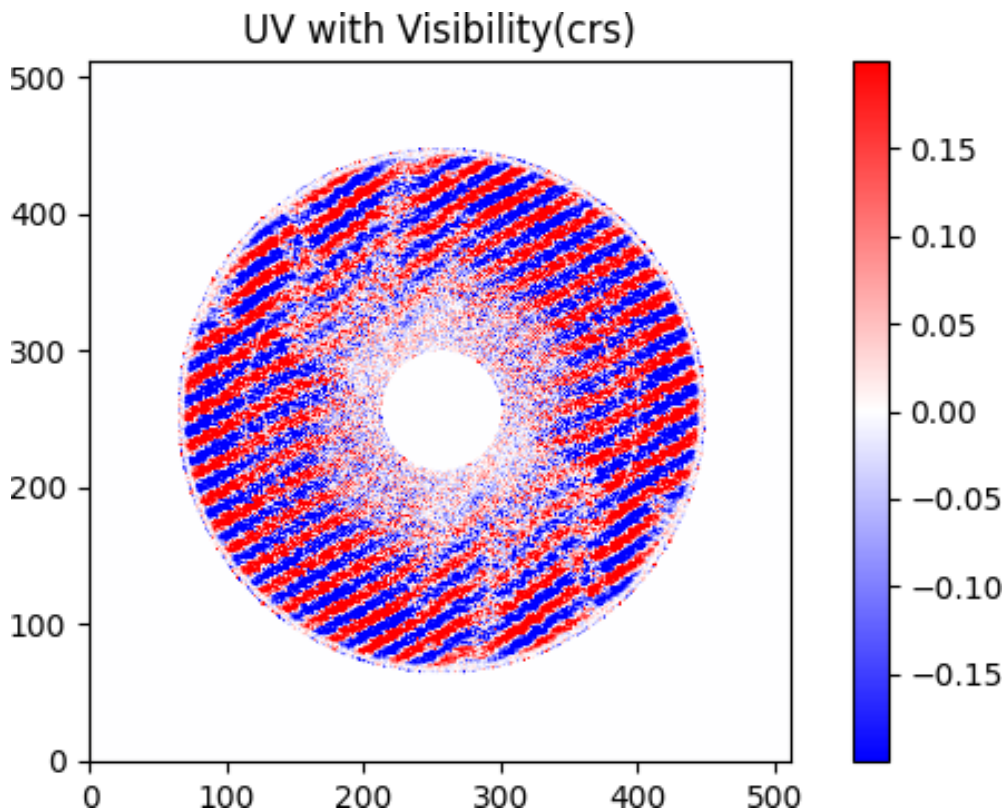


Figure 21: UV map of W20-E15

Sampling board: SNAP 1 v4

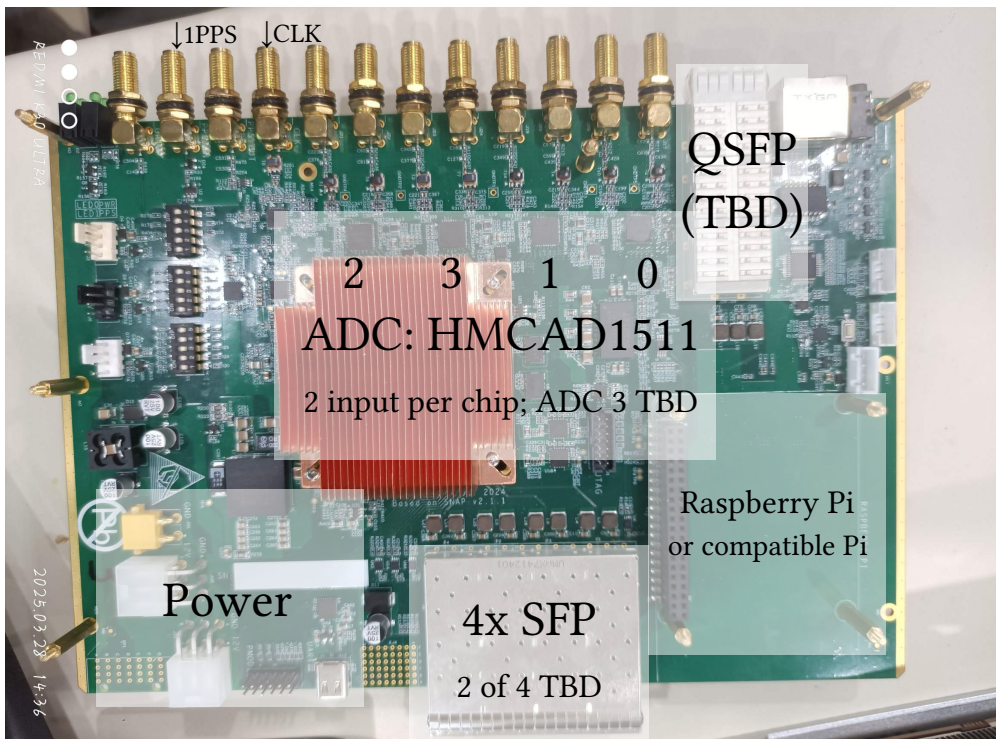


Figure 22: Overview of SNAP 1 v4

- hardware developed by collaborating company
- **4 × HMCAD1511**, interleaved ADCs
- **4 × 10 GbE, matches number of ADCs**
- removed freq. synthesizer & zdok connector
- **compatible with firmware of SNAP 1 v2**
- max data rate per board:
  - 8 × 500 Msps
  - 4 × 1 Gsps
- but firmware support for new hardware resource TBD (collaboration needed)
- price: < 10000, please contact Prof. Youling Yue if interested

数据采集卡: AiSense PG390

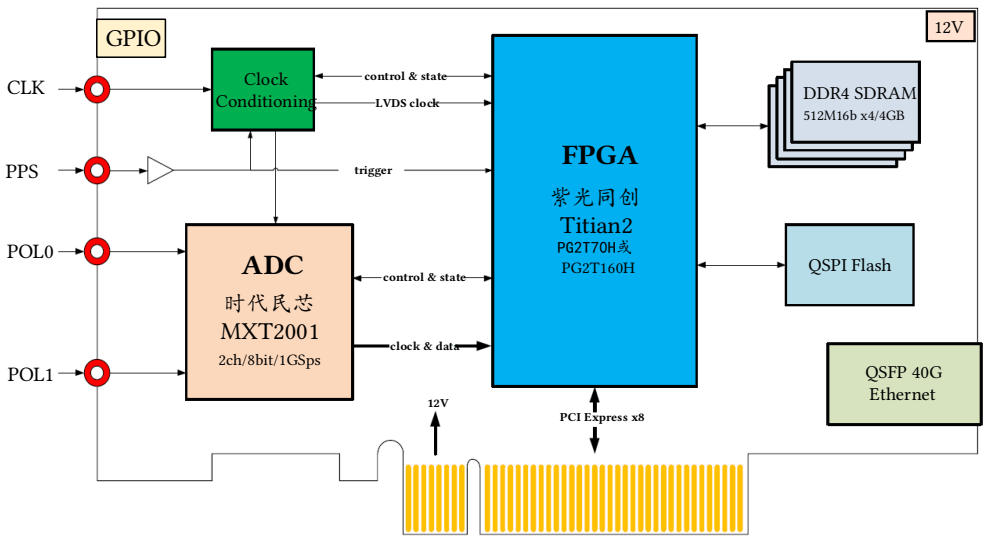


Figure 23: AiSense PG390 天文数据采集卡的框图

- 由合作公司研制
- **全国产解决方案**: FPGA (紫光同创), ADC (时代民芯), DDR4 内存 (长鑫)
- ADC: 1 × 时代民芯 MXT2001, 非交织采样
- 两种工作模式: **可用作 PCIe 采集卡, 也可独立工作并由网口输出数据**
- ≥ 2 × 10 GbE, 与 ADC 数据流个数匹配
- PCIe 3.0 x8
- 最大输出数据流量 (若考虑网络):
  - 2 × 1 Gsps; 1 × 2 Gsps (?)
- 电路板设计, FPGA 固件, 内核驱动与用户态运行库的源码均已获得, 可自行修改
- 价格: 目前较贵, 超过 SNAP 1 v4 的 1.5 倍

数据采集卡: AiSense PG390

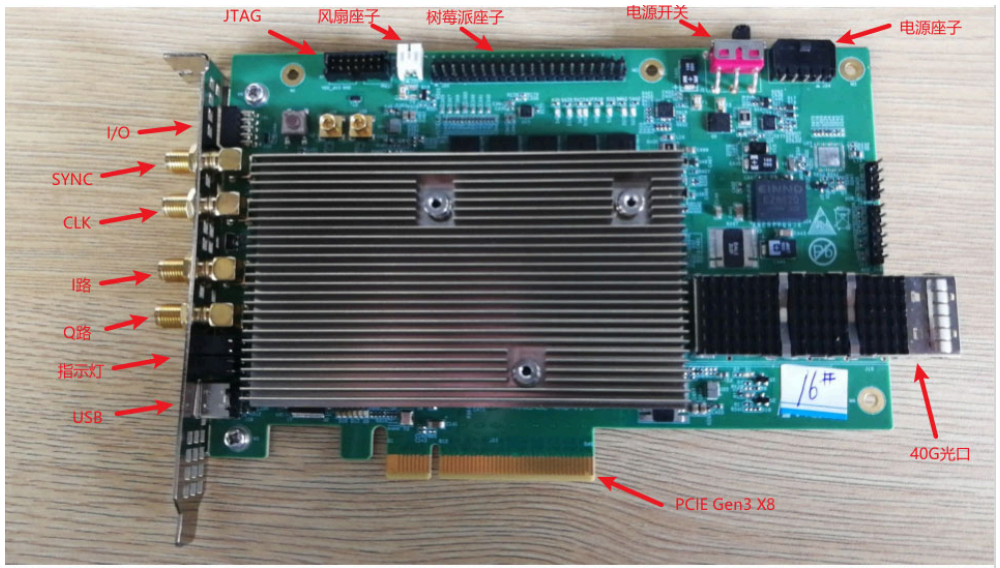


Figure 24: AiSense PG390 天文数据采集卡的实物图

- 由合作公司研制
- **全国产解决方案**: FPGA (紫光同创), ADC (时代民芯), DDR4 内存 (长鑫)
- ADC: 1 × 时代民芯 MXT2001, 非交织采样
- 两种工作模式: **可用作 PCIe 采集卡, 也可独立工作并由网口输出数据**
- ≥ 2 × 10 GbE, 与 ADC 数据流个数匹配
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- 最大输出数据流量 (若考虑网络):
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- 价格: 目前较贵, 超过 SNAP 1 v4 的 1.5 倍

Sampling board: RFSoC xczu27dr

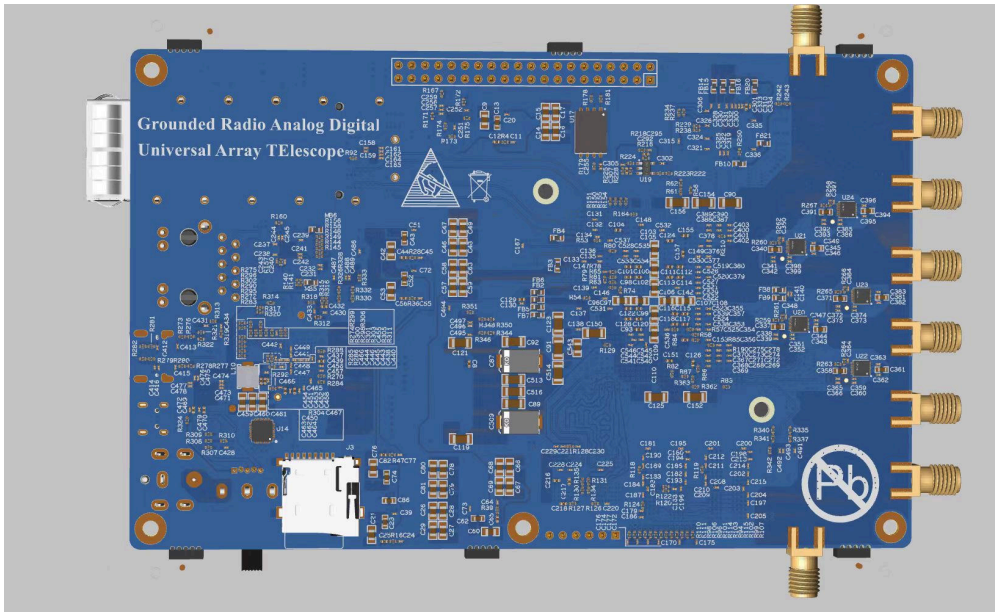


Figure 25: Design rendering of G.R.A.D.U.A.TE

- "Grounded Radio Analog Digital Universal Array TElescope (G.R.A.D.U.A.TE)"
- developed by Junhua Gu, Faxin Shen et al.
- first 5 sample boards manufacturing
- RFSoC xczu27dr, from obsolete mobile communication base station devices
- up to 4 × 4.096 Gsps ADC & up to 4 × 6.554 Gsps DAC; 1 × 100 GbE
- can upgrade to 8 × ADC, 8 × DAC, 2 × 100 GbE if it gains interest
- Price: estimated $\lesssim$ 10k, possibly $\ll$ 10k
- reference price for similar products: tq47dr 50k-70k, another 47dr 50k, ZCU111 120k

Wideband backend based on RFSoC ZCU111 / xczu47dr / xczu27dr

- not using CASPER Matlab + Vivado workflow, but uses IPs from CASPER (e.g. casper100g)
- current design: 8 data streams per board, 2.56 Gsps or 3.20 Gsps, 8 bit (12 bit TBD), send baseband to server using 2 × 100GbE; other processing procedures on GPU
- development at very early stage

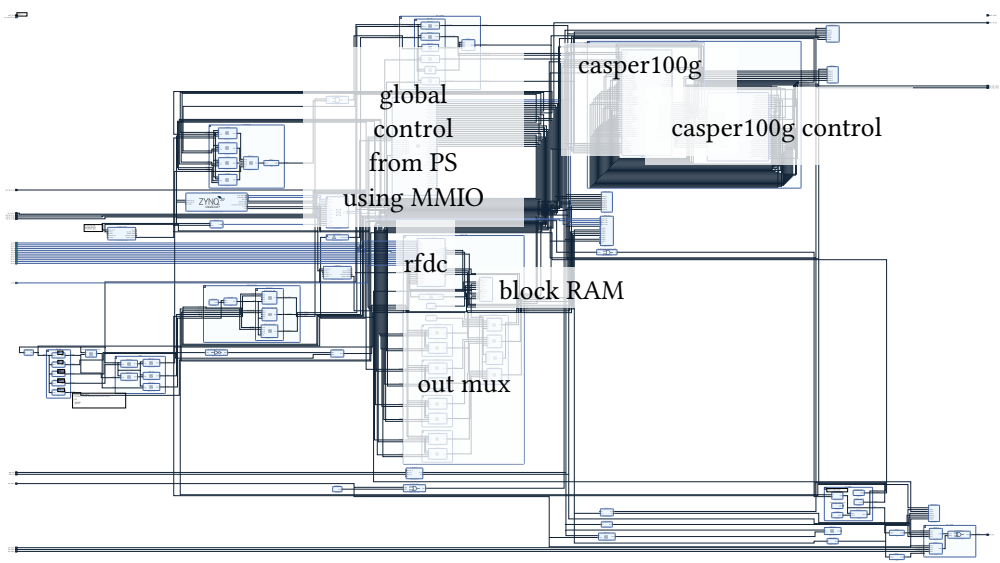


Figure 26: Block Design of firmware

Conclusion & Future work

- waiting for analog beamforming...
- detected pulsar using 21CMA-DBF on single station, E03 & W09
- implemented GPU-based & RDMA-based distributive correlator
- imaging and calibration of 21CMA data working-in-progress
- preliminary beamforming of 2 $\times$ 21CMA-DBF stations, covered area near PSR B0329+54 & get some S/N variance; will test other 2 DBF stations when availble
- some new sample boards: SNAP 1 v4, AiSense PG390, RFSoC xczu27dr "G.R.A.D.U.A.TE"; some are considered for future upgrade of 21CMA pulsar backend
- developing wideband backend based on RFSoC ZCU111 / xczu47dr / xczu27dr

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